IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Shunpei Yamazaki, et al. Art Unit : 2813
Serial No. : 09/451,665 Examiner : Laura Schillinger
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Title : SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

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SUBMISSION OF VERIFIED ENGLISH TRANSLATION

Supplemental to the reply filed February 14, 2006, Applicants submit herewith the verified English translation of priority application No. 07-090157 along with the verification of translation.

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In re Patent Application of:	)
Shunpei YAMAZAKI et al.	)
Application No.: 09/451,665	) Examiner:
Filed: November 30, 1999	) L. Schillinger
For: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF	) Group Art Unit:) 2813

VERIFICATION OF TRANSLATION

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Sir:

I, Yuri Taniguchi, C/O Semiconductor Energy Laboratory Co., Ltd. 398, Hase, Atsugi-shi, Kanagawa-ken 243-0036 Japan, a translator, herewith declare:

that I am well acquainted with both the Japanese and English Languages;

that I am the translator of the attached translation of the Japanese Patent Application No. 7-090157 filed on March 23, 1995; and

that to the best of my knowledge and belief the following is a true and correct translation of the Japanese Patent Application No. 7-090157 filed on March 23, 1995.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: this 7 day of March

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Name: Yuri Taniguchi

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[Reference Number] P002968-01

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[Title of the Invention] SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

[Number of Claims] 14

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[List of Attachment]

[Attachment] Specification 1

[Attachment] Drawing 1

[Attachment] Abstract 1

[Name of Document] Specification

[Title of the Invention] SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

[Scope of Claims]

[Claim1]

A semiconductor device having a plurality of thin-film transistors formed with crystalline silicon on a substrate having an insulating surface,

wherein the plurality of thin-film transistors includes a thin-film transistor having a P-type or N-type dopant in a channel formation region, and a thin-film transistor having no P-type or N-type dopant in a channel formation region practically.

[Claim 2]

A semiconductor device having a plurality of thin-film transistors formed with crystalline silicon on a substrate having an insulating surface,

wherein at least one of the plurality of thin-film transistors has a different concentration of a P-type or N-type dopant in a channel formation region from the other thin-film transistors.

[Claim 3]

The semiconductor device according to Claim 2, wherein a P-type dopant includes boron.

[Claim4]

A semiconductor device having a plurality of thin-film transistors formed with crystalline silicon on a substrate having an insulating surface,

wherein at least one of the plurality of thin-film transistors has a P-type or N-type dopant in a channel formation region, the dopant being a different kind from a

dopant included in channel formation regions of the other thin-film transistors.

[Claim 5]

A semiconductor device having a plurality of thin-film transistors formed with crystalline silicon on a substrate having an insulating surface,

wherein at least one of the plurality of thin-film transistors has a different threshold voltage (V_{th}) from the other thin-film transistors.

[Claim 6]

The semiconductor device according to Claims 2, 4, and 5, wherein a dopant in the channel formation region exists with a concentration of 5×10^{15} atoms/cm^3 to 5×10^{17} atoms/cm^3.

[Claim 7]

A method for manufacturing a semiconductor device, in doping a channel of a thin-film transistor, comprising the steps of:

forming a silicon film over one surface of a substrate having an insulating surface;

forming a control film having distribution in thickness intentionally over the silicon film; and

implanting a dopant into the control film and silicon film.

[Claim 8]

A method for manufacturing a semiconductor device, in doping a channel of a thin-film transistor, comprising the steps of:

forming a silicon film over one surface of a substrate having an insulating surface;

forming a control film having distribution in thickness intentionally over the

silicon film;

implanting a dopant into the control film and silicon film;

removing the control film; and

irradiating the silicon film with a laser light or light having a similar intensity to the laser light.

[Claim 9]

A method for manufacturing a semiconductor device, in doping a channel of a thin-film transistor, comprising the steps of:

forming a silicon film over one surface of a substrate having an insulating property;

forming a control film having distribution in thickness intentionally over the silicon film;

implanting a dopant into the control film and silicon film;

removing the control film; and

irradiating the silicon film with an excimer laser light.

[Claim 10]

A method for manufacturing a semiconductor device, in doping a channel of a thin-film transistor, comprising the steps of:

forming a silicon film over one surface of a substrate having an insulating property;

forming a control film over the silicon film;

forming a resist over the control film;

patterning the resist into a desirable shape; and

implanting a dopant into the control film and silicon film.

[Claim 11]

A method for manufacturing a semiconductor device, in doping a channel of a thin-film transistor, comprising the steps of:

forming a silicon film over one surface of a substrate having an insulating property;

forming a control film over the silicon film;

forming a resist over the control film;

patterning the resist into a desirable shape;

implanting a dopant into the control film and silicon film

removing the resist and the control film; and

irradiating the silicon film with a laser or light having a similar intensity to the laser.

[Claim 12]

The method for manufacturing a semiconductor device according to Claims 7 to 11, wherein the control film is a silicon oxide film.

[Claim 13]

A semiconductor device comprising:

thin film transistors having two or more different threshold voltages on the same substrate in a thin-film semiconductor integrated circuit,

wherein a thin-film transistor having a higher threshold voltage than that of a CMOS circuit is connected to a source electrode of a P-channel thin-film transistor and a source electrode of an N-channel thin-film transistor of the CMOS circuit formed on the substrate.

[Claim 14]

A semiconductor device wherein a plurality of pixels each connected to a thin-film transistor is arranged in matrix,

wherein a gate line drive circuit and a plurality of gate lines connected to the gate line drive circuit are provided,

wherein each of the gate lines is connected to the plurality of the thin-film transistors, and

wherein thin-film transistors that are more distant from the gate line drive circuit has a lower threshold voltage among the plurality of thin-film transistors connected to one gate line.

[Detailed Description of the Invention]

[0001]

[Technical Field to which the Invention pertains]

The present invention relates to reduction of power consumption of a thin-film semiconductor integrated circuit constituted of crystalline silicon. The invention also relates to reduction of power consumption of a drive circuit of an active matrix display device that is constituted of crystalline silicon.

The invention also relates to an ion doping technique for a semiconductor material, and a manufacturing method of a semiconductor and a semiconductor device using it.

Further, the invention relates to reduction of a leak current while a thin-film transistor (hereinafter abbreviated as TFT (Thin Film Transistor)) is OFF.

[0002]

[Related Art]

In recent years, studies have been actively made of the active matrix display device using a liquid crystal. In the active matrix display device, a switching element is provided for each pixel and a signal coming from an image signal line is supplied to each pixel by the above switching element.

Although previously thin-film transistors (TFT) using an amorphous silicon semiconductor were used as the switching element, in recent years, TFTs have been developed which use a silicon semiconductor having crystallinity (including crystal components) with a high operation speed.

[0003]

However, in a TFT using crystalline silicon, the leak current (OFF-current)

that flows when the gate electrode is reversely biased is larger than in a TFT using an amorphous silicon semiconductor.

The cause is believed to be due to the existence of crystal grain boundaries, which is the biggest problem because it increases the characteristics and power consumption of a circuit constituting an active matrix display device with the use of crystalline silicon.

In the case of an N-channel TFT, when V_{GS} (source-gate voltage of the TFT) is negatively biased, a leak current is determined by currents flowing through PN junctions that are formed between a P-type layer that is induced in the surface of a semiconductor thin film and N-type layers of source and drain regions. Because of many traps existing in the semiconductor thin film (particularly in grain boundaries), these PN junctions are incomplete, likely causing a junction leak current.

The reason why the leak current increases as the gate electrode is negatively biased more deeply is that the carrier concentration of the P-type layer formed in the surface of the semiconductor thin film increases, which narrows the energy barrier width of the PN junction, which causes an electric field concentration, resulting in increase of the junction leak current.

[0004]

The leak current that is caused as the above strongly depends on the source/drain voltage. It is known that the leak current rises sharply as the voltage applied between the source/drain of a TFT is increased. For example, in the case where voltage of 5 V is applied between a source/drain, and the case where voltage of 10 V is applied, the latter leak current may be 10 times larger or more than the former, rather than 2 times in some cases.

The above nonlinearity also depends on the gate voltage. In general, the difference between the two cases is remarkable when the reverse bias value of the gate electrode is large (in an N-channel TFT, when a larger negative voltage).

[0005]

[Problem to be Solved by the Invention]

Typical examples of products using the active matrix display device include a notebook-type personal computer and a portable information terminal. However, in those products at present, the active matrix display device is responsible for most of the total power consumption. Therefore, from the need for a long-term driving by a battery, it is desired to reduce the power consumption of the active matrix display device.

However, even where a peripheral drive circuit of an active matrix display device is constituted of CMOS (Complementary Metal-oxide Semiconductor) TFTs, large leak currents flow even if the P-channel TFTs are in an OFF state, making the power consumption of the entire circuit large.

[0006]

In the case of forming a high-resolution, large-screen type active matrix display device, long gate lines of the screen cause a problem that there is a delay until the TFT of a selected pixel is turned ON. A wiring resistance R_{wire} and a wiring capacitance C_{wire} of a gate line can be represented approximately as follows:

$$R_{wire} = \rho \cdot L/(W \cdot T)$$

$$C_{wire} = \varepsilon_{ox} \cdot W \cdot L/H$$

ρ: resistivity of a wiring material

L: wiring length

W: wiring width

T: wiring film thickness

ε_{ox}: dielectric constant of a field oxide film.

Herein, a delay t_{wire} of a signal due to a wiring line, which is equal to a time constant RC, is expressed as follows

$$t_{wire} = R_{wire} \cdot C_{wire} = \rho \cdot \varepsilon_{ox} \cdot L^2/(T \cdot H).$$

This equation indicates that the signal delay due to a wiring line is proportional to the square of the wiring length.

Conventionally, the signal delay due to a wiring line is prevented by reducing the wiring length of gate lines by providing gate line drive circuits on both sides of the active matrix display device. However, it is not sufficient.

[0007]

[Problem to be Solved by the Invention]

In view of the above, an object of the present invention is to provide a structure in which power consumption of a thin-film semiconductor integrated circuit formed on crystalline silicon, in particular, a peripheral drive circuit of an active matrix liquid crystal display device is reduced.

Another object of the invention is to provide a structure of a pixel-switching thin-film transistor of an active matrix liquid crystal display in which a signal delay due to a wiring line can be prevented.

A further object of the invention is to provide a method for forming thin-film transistors having different threshold voltages (V_{th}) on the same substrate.

[0008]

[Means for Solving the problem]

As described above, the leak current in a CMOS circuit as a thin-film semiconductor integrated circuit formed on crystalline silicon can be reduced by decreasing the source/drain voltage.

To this end, according to the invention, a P-channel TFT and an N-channel TFT are connected to the source electrodes of a P-channel TFT and an N-channel TFT of a CMOS circuit, respectively. The threshold voltages of the connected P-channel and N-channel TFTs are made higher than those of the CMOS circuit. Thus, by making the connected P-channel and N-channel TFTs in an OFF state, the CMOS circuit can be separated from a power supply when the CMOS circuit is not in use.

Since the threshold voltage of the CMOS circuit is lower, the leak current of the CMOS circuit is reduced. Thus, the power consumption of an integrated circuit constituted of thin-film transistors can be reduced.

[0009]

In addition, pixel TFTs are constructed such that the threshold voltage of each TFT is determined in consideration of a voltage drop due to a wiring resistance of a gate line of an active matrix display device. That is, the thin-film transistors are constructed such that a thin-film transistor more distant from a gate line drive circuit has a lower threshold voltage. As a result, the gate voltage of a pixel TFT that is about to be driven is lower than the conventional. Therefore, the charging time of one wiring capacitance of a gate line can be shortened, so that pixel TFTs provided distant from the gate line drive circuit can be turned ON in shorter time than the conventional.

[0010]

Further, in this manner, a description will be made of a method for making

each of threshold voltages of a plurality of thin-film transistors formed on the same substrate different from one another.

In recent years, it has been attempted to perform doping in the channel region of a thin-film transistor (TFT). Hereinafter, this technique is called channel doping.

The channel doping enables control of V_{th} (threshold voltage). Although inherently V_{th} should be 0 V (actually, I_D (drain current) approximately has a minimum value when V_G (gate voltage) is 0 V), it may deviate much from 0 V when a semiconductor material is processed to enhance its crystallinity or improve its uniformity. Other factors may also deviate V_{th}. In any case, deviation of V_{th} can be made about 0 V by channel doping.

[0011]

Whether an N-type dopant (a doped semiconductor exhibits N-type conductivity) or a P-type dopant (a doped semiconductor exhibits P-type conductivity) is used depends on that V_{th} has deviated either to the negative side or the positive side. Further, the dose of channel doping is changed in accordance with the amount of V_{th} deviation. That is, no matter how V_{th} deviates, V_{th} can be made about 0 V by adjusting the dose of channel doping. Further, fine adjustment of V_{th} can be also done by adjusting the dose.

In general, the dose of channel doping is lower than the dose implanted in source drain.

Annealing is performed after doping to repair lattice defects that have been produced by a large amount of dopant implanted into a semiconductor material.

[0012]

A method for intentionally making V_{th} of a plurality of thin-film transistors

different from one another will be described below. For varying Vth in elements, doses in doping the channel regions of the transistors may be changed, as described above.

[0013]

Fig. 2 shows distribution of the dose of a dopant implanted into a silicon film by doping.

To control the dose in each of thin-film transistors, the nature of the dose after doping which enters a doped object as in the distribution in Fig.2 is used. In Fig. 2, the vertical axis represents the dose and the horizontal axis represents the depth from the surface of a doped object.

As Fig. 2 shows, the dose distributes to have a range of about three-digit number to the depth direction.

With this distribution, in forming a thin-film transistor, a control film, for instance, a silicon oxide film, that can be stripped off in a later step is formed on the surface of the channel region of the thin-film transistor, and doping is performed from the above of it. Thus, dose amount of an impurity introduced into the channel region can be adjusted by the thickness of the control film.

[0014]

In this method, a concentration distribution is provided in the same substrate in doping the same kind of dopant. However, this can move V_{th} only in one direction (i.e., positive or negative direction).

This problem can be solved by implanting different kinds of dopants into different regions.

Further, to produce both of thin-film transistors in which V_{th} is not shifted at all and those in which V_{th} is shifted, undoped regions and doped regions may be formed.

The above techniques of controlling V_{th} can be used not only to make V_{th} of each of thin-film transistors constituting a circuit different from one another, but also to eliminate differences and to make them uniform, when thin-film transistors have different V_{th} altough they are intended to be formed with the same V_{th}. Hereinafter, embodiments are described.

[0015]

[Embodiment]

[Embodiment 1]

In this embodiment, a channel doping step is inserted in a process of forming a plurality of thin-film transistors on the same substrate. In particular, this embodiment describes a manufacturing method of thin-film transistors having superior circuit characteristics.

More specifically, this embodiment relates to a technique of improving the characteristics of the entire circuit or reducing the power consumption of the entire circuit by making V_{th} values of transistors different from one anther by controlling V_{th} by use of a channel doping technique.

In this embodiment, a description will be made of a part of a process up until a channel doping step. After that, transistors can be formed by an ordinary method by using a silicon film produced by this embodiment.

[0016]

First, thin-film transistors in the midst of manufacture, i.e., before being to be doped are prepared. Thin-film transistors include a 500-Å-thick silicon film formed on a glass substrate (Corning 7059) and a 1,200-Å-thick silicon oxide film formed thereon. Naturally the thicknesses of these films may be set as desired.

The silicon oxide film is a control film for controlling the dose of a dopant to be implanted into a channel portion. The control film may be a silicon nitride film. Details will be described later.

The reason why the channel doping is performed at this stage is that the channel portion of a planar thin-film transistor is usually located under the gate electrode and therefore doping should be performed before formation of the gate electrode. The silicon film as used here means a film mainly made of silicon, and has an amorphous structure or a crystalline structure having crystal components such as a microcrystalline or polycrystalline structure.

[0017]

Next, a doping apparatus will be described briefly. Fig. 1 shows a schematic diagram of a doping apparatus.

Plasma is generated in a plasma source 501 in top of Fig. 1, and ions generated therein are accelerated by applying voltage in an ion acceleration region that is located under the plasma source. As shown in the figure, three places are provided to be applied voltage. They are called a deceleration voltage 504, an acceleration voltage 503, and an extraction voltage 502 respectively from the bottom in order. In an actual doping operation, voltages are applied from the bottom in order. A substrate holder 505 incorporates a heater to keep the substrate at an arbitrary temperature.

[0018]

An actual doping method is as follows. Boron is used as a dopant, here (Other dopants may be used; that is, the dopant is changed in accordance with the purpose.).

In this embodiment, a 5%-dilution diborane gas is used. A diborane gas is

introduced into the plasma source of the doping apparatus, and thin-film transistors in the midst of manufacture, i.e., before doping is set on the substrate holder 505 in Fig. 1. At this time, the heater incorporated in the substrate holder 505 is kept so as to be 50 to 500°C. By keeping a high temperature, the activation of a semiconductor substrate under doping can be accelerated.

[0019]

Subsequently, the ion acceleration region is vacuumized, and the diborane gas is introduced into the acceleration region from the plasma source. Immediately after application of a deceleration voltage of -1 kV, an acceleration voltage of 27 kV is applied and the state is maintained for 5 seconds. Finally, an extraction voltage is applied by continuously raising to 3 kV in 1 second.

With the above process, boron is implanted into the surface of a silicon oxide film, which is a control film, to the silicon film with a profile shown in Fig. 2. As seen from the profile of the depth of 1200 Å to 1700 Å in Fig. 2, it is known that a dopant of 6×10^{16} atoms/cm^3 to 6×10^{17} atoms/cm^3 is included. This profile is according to BHx.

On the other hand, a profile from the surface to 1,200 Å shows a mountainous shape profile, and it is known that dopant of 7×10^{18} atoms/cm^3 at a maximum is included.

[0020]

This mountainous profile is due to B_2H_y. This portion does not influence the characteristics of TFTs at all, no matter how much dopant is introduced, because this portion is in the silicon oxide film.

The reason why the silicon oxide film is formed is to put dopant at a low dose of about 1×10^{17} atoms/cm^3 into the silicon film (It is difficult to directly implant the dose of about 1×10^{17} atoms/cm^3 with existing doping apparatuses.).

The above dose values are presented just for reference, and a desired dose may be implanted in accordance with a purpose. Experiments conducted by the applicants have revealed that, in channel doping, a lower dose may be implanted than the dose implanted into source drain, and that the threshold voltage control can be performed favorably if the dose falls within a range of 5×10^{15} atoms/cm^3 to 5×10^{17} atoms/cm^3.

[0021]

By applying the above-described doping technique, the dose implanted into a channel region can be made different from one transistor to another. Techniques necessary for that will be described below.

[0022]

1. A method for forming elements to which channel doping is not performed at all and elements to which channel doping is performed on the same substrate.

This can be done simply by masking, during a doping, a region that is not required to be doped. Specifically, a resist is formed on the above-mentioned silicon oxide film, which is the control film, and then the resist is patterned. Since a region under the resist is not doped, a portion to be doped and a portion not to be doped can be discriminated from each other. After the doping, the silicon oxide film and the resist film are removed. Anything can be used as long as it has the same function as the resist, in this case.

[0023]

2. A method for implanting the same kind of dopant into regions at different concentrations.

For this, it is preferable to vary the thicknesses of silicon oxide films for respective regions, and conduct doping thereon. Because, with this method, the dose

distributes as Fig. 5 can be obtained. Fig. 5 shows a distribution of the dose.

The doses are different markedly at points A and B in Fig. 5.

Specifically, a resist is provided on the silicon oxide film, which is the control film, and the resist is patterned. After that, the silicon oxide film is etched to the desired thickness. Then, the silicon oxide films having different thicknesses in respective regions are made, after the resist is removed. Doping is conducted thereon.

[0024]

3. A method for implanting different kinds of dopants into respective regions.

Method 1 is utilized. Method 1 may be conducted two times, but it includes too many steps. Therefore, only a resist film is removed after the first doping, and a new resist film is formed. Then, second doping is conducted by conducting patterning which is different from the first one.

[0025]

Although the above three methods are the ones for conducting doping of different dopants in two regions, they may be used for three or more regions. These methods enable a finer control of V_{th} in each element.

After the doping, thermal annealing is performed to repair lattice defects that have been produced by a large amount of dopant implanted into a semiconductor material.

Thereafter, a silicon film obtained in the above manner is processed, and a gate insulating film, a gate electrode, source/drain electrodes, a passivation film, a pixel electrode, or the like are provided. Thus, thin-film transistors having different threshold voltages can be formed on the same substrate.

[0026]

[Embodiment 2]

A laser annealing step is inserted after the step shown in Embodiment 1, or instead of the thermal annealing. The purpose of the irradiation of the laser light is reduction of lattice defects in the silicon film, improvement of the crystallinity, and homogenization of distribution of the dopant over the entire substrate.

The silicon oxide film is removed by etching before the laser annealing.

First, a description will be made of a laser apparatus. Fig. 3 shows the conceptual diagram of a laser annealing apparatus used in this embodiment. The laser light is emitted by an oscillator 2. KrF excimer laser light (wavelength: 248 nm; pulse width: 25 ns) is emitted from the oscillator 2. Obviously, other excimer lasers and further other types of lasers may also be used.

[0027]

The laser light emitted from the oscillator 2 is amplified by an amplifier 3, after passing full-reflection mirrors 5 and 6, and introduced into an optics 4 after further passing full-reflection mirrors 7 and 8. Immediately before entering the optics, the laser light beam has a rectangular shape of approximately 3 × 2 cm^2; however, the laser light beam is processed by the optics 4 to be a long and narrow beam (linear beam) of approximately 10 to 30 cm in length and 0.1 to 1 cm in width. The energy of the laser light that has passed the optics 4 is 1,000 mJ/shot at a maximum.

[0028]

The reason for processing the laser light into the long and narrow beam is to improve its processability. In other words, the linear beam output from the optics 4 passes a full-reflection mirror 9, and a sample 11 is irradiated with it. Since the width of the beam is longer than the width of the sample, the entire sample can be irradiated with

the laser light by moving the sample in one direction. Therefore, a sample stage and a driving device 10 are simple in structure and easy to maintain. In addition, an alignment operation (alignment) in setting the sample is also easy.

[0029]

The sample stage 10 which is to be irradiated with the laser light is controlled by a computer, and is designed so as to move perpendicularly to the linear laser light. Under the stage 10, a heater is incorporated to keep the sample at a prescribed temperature during laser light irradiation.

[0030]

An optical path inside the optics 4 is shown in Fig. 4. The laser light that has been input to the optics 4 passes through a cylindrical concave lens A, a cylindrical convex lens B, and horizontal flyeye lenses C and D, so that the laser light changes from the original Gaussian distribution to a rectangular distribution. Then, it passes through cylindrical convex lenses E and F and then through a mirror G (which corresponds to the mirror 9 in Fig. 3), thus, it is focused by a cylindrical lens H, and finally irradiates the sample.

[0031]

A specific laser irradiation is conducted as follows. The laser beam is shaped into a rectangular form by the beam shape converting lenses to provide a beam area of 125 mm × 1 mm on the irradiation portion. The sample is mounted on the stage 10, and by moving the stage at a rate of 2 mm/s, its entire surface is irradiated.

As for the laser light irradiation conditions, two-step irradiation consisting of preliminary irradiation of 150 to 250 mJ/cm^2 and main irradiation of 200 to 380 mJ/cm^2 is employed, and the pulse rate is set at 30 pulses/s. The reason for employing the two-step

irradiation is to minimize degradation of the uniformity of a film surface due to the laser irradiation, thereby producing a film having better crystallinity.

[0032]

The substrate temperature is kept at 200°C during the laser light irradiation to reduce the speed of increase and decrease of the substrate surface temperature due to the laser. Although in this embodiment the substrate temperature is set at 200 °C, in the actual operation, the most suitable temperature for laser annealing is selected from the range of 100 °C to 600 °C. No particular atmosphere control is performed, and the irradiation is conducted in the air.

Instead of using laser light, strong light equivalent to laser light, for instance, infrared ray may be applied by using an infrared ray lamp.

[0033]

[Embodiment 3]

As a shift register constituting a drive circuit of an active matrix display device, a circuit which can reduce leak current is shown in Fig. 6.

One output signal of the shift register is produced by one timing generation circuit and two power supply control circuits.

FF_{i-2} to FF_{i+2} are timing generation circuits, whose circuit diagram is shown in Fig. 7. Each of the timing generation circuits consists of one clocked inverter that is constituted of thin-film transistors having a low threshold voltage and two inverters each constituted of thin-film transistors having a high threshold voltage.

These thin-film transistors having different threshold voltages are ones that have been manufactured by the method in Embodiment 1.

The timing generation circuits generate scanning timing or image signal output

timing of the active matrix display device.

A signal clk in the figure is an operation clock signal for the timing generation circuit, and *clk is a signal obtained by logically inverting the clk. Signals Q_{i-2} to Q_{i+2} in the figure are the output signals of the timing generation circuits, which becomes the output signals of the shift register. $*Q_{i-2}$ to $*Q_{i+2}$ are signals obtained by logically inverting the signals Q_{i-2} to Q_{i+2}.

[0034]

VC_{i-2} to VC_{i+2} are power supply control circuits. The circuit diagram is shown in Fig. 8. The power supply control circuit is an SR latch consisting of one two-input NAND having a high threshold voltage and one three-input NAND having a high threshold voltage. The power supply control circuit controls separation from a power supply of the timing generation circuit.

In the figure, PON_{i-2} to PON_{i+2} are signals for turning ON/OFF a P-channel TFT that is connected to the timing generation circuit. In the figure, NON_{i-2} to NON_{i+2} are signals for turning ON/OFF an N-channel TFT that is connected to the timing generation circuit. *RESET in the figure is a signal that is input for a certain period after the power-on to prevent the SR latch of the power supply control circuit from producing contradictory outputs and thereby fixing the logic, after the power-on of an active matrix display device.

[0035]

The operation of the circuit will be described below.

When an input pulse is input to the timing generation circuit i, the output signals Q_i and $*Q_i$ that are clock-synchronized are output by the clocked inverter. The output signal Q_i serves both as a timing signal for the active matrix display device and an

input pulse for the timing generation circuit (i+1) of the next stage.

The output signal $^*Q_i$ is input to the power supply control circuit (i+2), and makes output signals PON_{i+2} and NON_{i+2} active. As a result, the timing generation circuit (i+2) is connected to the power supply.

At the same time, the output signal $^*Q_i$ is input to the power supply control circuit (i–2), which makes output signals PON_{i-2} and NON_{i-2} non-active. As a result, the timing generation circuit (i–2) is separated from the power supply.

[0036]

In this embodiment, when the shift register produces n-stage outputs, (n+2) timing generation circuits and (2n-4) power supply control circuits exist. The reasons are as follows. To perform power supply control (separation from the power supply) of the timing generation circuits (n–1) and n, timing generation circuits (n+1) and (n+2) are needed. In addition, to prevent oscillation of the shift register after the power-on, a power supply control circuit is not included in timing generation circuits 1, 2, (n+1), and (n+2).

[0037]

As the above, by using the TFTs having a high threshold voltage, in the circuit which does not output a signal of the shift register, the clocked inverter of the timing generation circuit is separated from the power supply. Further, since the TFTs constituting the clocked inverter have a lower threshold voltage than the TFTs connected to the power supply, the leak current can be reduced than the conventional. In addition, since the inverter of the timing generation circuit holds the output signal, no leak current flows, which contributes to reduction of the power consumption of the active matrix display device.

[0038]

[Embodiment 4]

In Embodiment 4, an example of an arrangement of pixel TFTs having increased switching speed in an active matrix display device is shown.

Fig. 9 shows a schematic diagram of a gate line drive circuit and pixel TFTs of an active matrix display device according in Embodiment 4.

A gate line drive circuit 901 is constituted by connecting a plurality of inverters.

TFT_1 to TFT_n are N-channel pixel TFTs, which have been manufactured according to the method of Embodiment 1 so that threshold voltages V_{th1} to V_{thn} of the respective TFTs satisfy a relationship of $V_{th1} \geq V_{th2} \geq .... \geq V_{th(n-1)} \geq V_{thn}$.

That is, a pixel TFT more distant from the gate line drive circuit has a lower threshold voltage.

With the above configuration, a TFT more distant from the gate line drive circuit can have a lower gate voltage. As a result, the charging time of the wiring capacitance of a gate line can be shortened, so that the pixel TFTs provided distant from the gate line drive circuit can be turned ON in shorter time than in the conventional.

Thus, in the active matrix display device, the gate line drive circuit can turn on the pixel TFTs in shorter time than in the conventional.

[0039]

[Effect of the Invention]

As described above, according to the invention, it becomes possible to reduce leak current and power consumption of a thin-film semiconductor integrated circuit made of crystalline silicon, in particular, a peripheral drive circuit of an active matrix display device.

In addition, TFTs formed on the same substrate, which has two or more different threshold voltages can be formed.

Further, in pixel TFTs of the display portion of an active matrix display device, pixel TFTs provided distant from a gate line drive circuit can be turned ON in shorter time than in the conventional.

In other words, the invention makes it possible to improve the circuit characteristics by controlling the threshold voltages V_{th} of thin-film transistors made of crystalline silicon.

[BRIEF DESCRIPTION OF THE DRAWINGS]

[Fig. 1] A schematic diagram showing a doping apparatus.

[Fig. 2] A diagram showing distribution of the dose of a dopant implanted into a silicon film by doping;

[Fig. 3] A schematic diagram showing a laser annealing apparatus used in Embodiment 2.

[Fig. 4] A diagram showing an optical path inside an optics 4 in Fig. 3

[Fig. 5] A diagram showing distribution of the dose.

[Fig. 6] A schematic diagram showing a drive circuit of an active matrix display device in Embodiment 3.

[Fig. 7] A circuit diagram of timing generation circuits constituting a drive circuit in Embodiment 3.

[Fig. 8] A circuit diagram showing a power supply control circuit constituting a drive circuit in Embodiment 3.

[Fig. 9] A schematic diagram showing a gate line drive circuit and pixel TFTs of an active matrix display device in Embodiment 4.

[Numeral Reference]

2: oscillator

3: amplifier

4: optics

5 to 9: full-reflection mirrors

10: stage

501: plasma source

502: extraction voltage

503: acceleration voltage

504: deceleration voltage

505: substrate holder

601 to 605: timing generation circuits

606 to 610: power supply control circuits

901: gate line drive circuit

[Document Name] Abstract

[Summary]

[Problem] It is an object of the present invention to provide a structure in which power consumption of a peripheral drive circuit of an active matrix liquid crystal display device is reduced, and a signal delay due to a wiring line is prevented in a pixel-switching thin-film transistor. Further, it provides a method for forming a thin-film transistor having different threshold voltages (V_{th}) on the same substrate, for that.

[Structure] A TFT having a high threshold voltage is connected to the source electrode of each TFT that constitutes a CMOS circuit. Further, pixel TFTs are constructed such that a thin-film transistor more distant from a gate line drive circuit has a lower threshold voltage. Moreover, a control film that is removable in a later step is formed on the surface of the channel region of a TFT, and doping is performed from above the control film.

[Selected drawing] Fig. 5